REMARKS

In the Office Action, the Examiner allowed Claims 11, 13, 15 and 16 were allowed. Claims 1, 3-7, 9, 10, 12 and 14, which are the other pending claims, under 35 U.S.C. §103 as being unpatentable over the prior art, principally U.S. Patents 6,211,849 (Sasaki, et al.), 6,658,666 (Arsenault) and 5,148,263 (Hamai).

With respect to the rejected Claims, Claims 1, 4, 6 and 7 were rejected as being unpatentable over Sasaki, et al. in view of Arsenault and Hamai; and Claim 3 was rejected over Sasaki, et al. in view of Arsenault, and Hamai and further in view of U.S. Patent 5,623,519 (Babcock, et al.). Claim 5 was rejected as being upatentable over Sasaki, et al, Arsenault and Hamai, and further in view of U.S. Patent 5,801,674 (Shimizu); and Claim 9 was rejected over Sasaki, et al, Arsenault and Hamai, and further in view of U.S. Patent 5,825,777 (Komarek, et al.). Claim 10 was rejected over Arsenault in view of Sasaki, et al and Hamai; Claim 12 was rejected over Sasaki, et al. in view of Arsenault and U.S. Patent 6,335,778 (Kubota, et al.); and Claim 14 was rejected over Sasaki, et al. in view of Arsenault, Hamai, and U.S. Patent 6,204,864 (Jayavant).

Claims 1, 4, 6, 10, 12 and 14 are being amended to better define the subject matters of these claims. More specifically, each of these claims is being amended to describe the feature that each driver IC includes a controller for, or performs the step of, transmitting a wait bit block to a succeeding driver IC in the series in which the driver ICs are connected. Also, Claim 17, which is dependent from Claim 1, is being added to describe preferred features of the invention.

For the reasons discussed below, Claims 1, 3-7, 9, 10, 12, 14 and 17 patentably distinguish over the prior art and are allowable. The Examiner is, thus, requested to reconsider

and to withdraw the rejections of Claims 1, 3-7, 9, 10, 12 and 14 under 35 U.S.C. §103, and to allow these claims and new Claim 17.

The present invention, generally, relates to a liquid crystal display device. In this device, a driver interface and the individual driver ICs are connected together in series, either by a video signal line or by a transmission line, and in use, video signal data are transmitted to the driver ICs over those lines.

Sasaki teaches a driver IC's cascade connection method, however this reference does not disclose or suggest that a plurality of signals (video, clock, power source) is passed through metals of the driver ICs (see Fig 1 of Sasaki).

As examiner pointed out, Hamai shows an outside power pad being connected to an inside metal layer. However, Hamai only shows a discrete IC chip which has a multi-layered closed loop-pattern (power supply line pattern) connected to power pad, and this reference does not teach that a power feed line should be placed inside the driver ICs, which are cascade-connected.

A mask signal by Arsenault will be a local bit mask, and thus Arsenault does not suggest or teach that the mask signal is generated by a controller of driver ICs to forcibly set video data to '1' (wait bit block).

With particular regard to claim 1, Sasaki et al. does not show that the driver receives a digital packet signal including an input video signal and each driver IC includes a controller for generating a mask signal to mask video data output from the driver IC.

Arsenault et al. teaches how to filter incoming data by using a bit mask. However, the meaning of bit mask described Arsenault is different from the bit mask of the present invention. In the Arsenault system, an IRD has a local bit mask, which is comprised of a plurality of flags,

and performs a logical operation using the local bit mask and each incoming carousel mask to determine which objects to save.

In the embodiment of the present invention described in detail in the present application (see Figures 14 and 17), the bit mask operation means forcing the differential buffer output signal to become 1. Therefore, Arsenault et al. does not show a driver IC including a controller for generating a mask signal to force video data to become 1(Wait bit block).

With respect to claims 4, 6 and 10, here too, it is important to note that the meaning of bit mask disclosed in Arsenault et al. is different from the masking signal described in these Claims. The bit mask operation described in Claim 4, 6 and 10 forces the output bit block to become the wait bit block.

As to claim 12, again, the meaning of bit mask described by Arsenault et al. is different from the bit mask operation described in this claim. The latter bit mask operation forces the output bit block to become the wait bit block.

In addition, Kubota et al. does not show the way to transmit a synchronization pattern during a horizontal blanking period. According to the description in Col.9 Lines 39-46, the digital image signals are latched in the first memory LAT in a horizontal scanning period. Then,